# MERU UNIVERSITY OF SCIENCE AND TECHNOLOGY

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**UNIVERSITY EXAMINATIONS 2024/2025**

THIRD YEAR, FIRST SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRICAL AND ELECTRONIC ENGINEERING

**EET 3300: DIGITAL ELECTRONICS II**

**DATE: JANUARY 2025** **TIME: 2 HOURS**

**INSTRUCTIONS: Answer Question ONE and any other TWO questions.**
**: Show all your workings clearly**

**QUESTION ONE (30 MARKS)**

(a) Differentiate between saturated and non-saturated logic and enumerate two examples in each case. (3 Marks)

(b) Define the following terms in relation to digital logic families and explain their significance:

i. Power dissipation (1 Mark)
ii. Fan in and fan out (1 Mark)
iii. Propagation delay (1 Mark)
iv. Speed power product (1 Mark)

(c) Explain the following terms with regards to output configurations in TTL logic families:

i. Totem pole output (1 Mark)
ii. Open collector output (1 Mark)

(d) Draw the circuit implementation of the following logic functions using CMOS Logic:

i. AND gate (2 Marks)
ii. OR gate (2 Marks)
iii. Inverter (2 Marks)

(e) You are designing a control system for a factory that uses sensors to monitor machines. The system uses logic gates to process signals from the sensors and control actuators. The following details are provided: Number of sensors: 5, Fan-In of the logic gates: 4, Fan-Out of the logic gates: 6, Power Supply Voltage ($V_{CC}$): 3.3V, Average current per gate ($I_{CC}$): 5mA, Propagation delay per gate: 10 nanoseconds (ns), Maximum acceptable Speed-Power Product (SPP): 50 pJ. Determine the following:

i. Whether the logic gates with a fan-in of 4 sufficient to handle the 5 sensor inputs? If not, how many gates are needed? (1 Mark)

ii. The power dissipation for each logic gate. (1 Mark)

iii. the speed-power product (SPP) for each gate, and does it meet the requirement of 50pJ? (2 Marks)

iv. If each gate controls 3 actuators, how many more actuators can each gate drive without exceeding its fan-out limit? (2 Marks)

(f) A 4-bit Digital-to-Analog Converter (DAC) has an input voltage range of 0V to 8V.

i. Calculate the resolution of the DAC. (1 Mark)

ii. If the DAC operates at a clock frequency of 500 kHz, calculate the total conversion time for a 6-bit DAC and compare how the conversion time changes as the number of bits increases from 4 bits to 6 bits. (2 Marks)

(g) A TTL logic gate draws 2 mA when its output is HIGH and 3.5 mA when its output is LOW. Calculate the average power dissipation if the supply voltage is 5 V and the logic gate is operated on 50% duty cycle. (2 Marks)

(h) You are tasked with designing a complex control system for an industrial automation project. After evaluating different options, you are considering using Programmable Logic Devices (PLDs) instead of traditional Standard ICs for the implementation of large combinational logic circuits. Explain why PLDs would be a better choice in this scenario by providing at least four reasons to justify your decision. (4 Marks)

**QUESTION TWO (15 MARKS)**

(a) Describe the write operation in a DRAM cell. How does the capacitor store data and what role does the word line and bit line play in this process? (3 Marks)

(b) Using a PROM, implement the following Boolean function with two outputs given by the Boolean expressions: (4 Marks)

$$F_1(A1, A0) = \sum m(1, 2)$$

$$F_2(A1, A0) = \sum m(0, 1, 3)$$

(c) Design a combinational circuit using a PROM that reads the 3-bit temperature reading from the sensor and outputs the square of this value. The PROM will store the squared values for all possible sensor readings (0–7). Explain would you configure the PROM for this task, and what would the truth table look like for this setup? (8 Marks)

**QUESTION THREE (15 MARKS)**

(a) With the aid of a sketch, explain how a Binary Weighted D/A Converter works and derive the expression output voltage for a 4-bit DAC. (7 Marks)

(b) Table Q3(b) shows the truth table for Boolean functions X and Y to be implemented using a PAL. Obtain the following: (8 Marks)

i. Boolean expressions for X and Y

ii. Simplify expressions in (i) above using Karnaugh map and write the simplified expressions.

iii. Draw the PLA programming table for expressions in (ii)

iv. Draw the logic diagram of the combinational circuit implemented using PLA table in (iii)

| **Inputs** | | | **Outputs** | |
|---|---|---|---|---|
| ***A*** | ***B*** | ***C*** | ***X*** | ***Y*** |
| **0** | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 |

| | | | | |
|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

*Table Q3 (b)*

**QUESTION FOUR (15 MARKS)**

**(a)** Using suitable illustrations, highlight the key differences between the following PLDs

i. PROM (2 Marks)

ii. PLA (2 Marks)

iii. PAL (2 Marks)

(b) You're designing a simple traffic control system at an intersection, and you need to decide when the stoplights should change based on input from sensors that detect the presence of vehicles in different lanes. The sensors provide binary signals (0 or 1) for three conditions: cars in lane A, cars in lane B, and cars in lane C. You need to implement the control logic using a programmable array logic (PAL) chip to determine two important signals:

- Signal X: To control the stoplight for lane A.
- Signal Y: To control the stoplight for lane B.

Given the conditions:

- X should be triggered if there are cars in lane A and lane B, or if there are cars in lane A and no cars in lane C.
- Y should be triggered if there are cars in lane A and no cars in lane B, or if there are cars in lane B and no cars in lane C.

Implement this traffic control logic using PAL? (9 Marks)

**QUESTION FIVE (15 MARKS)**

(a) A 4-bit DAC is used in a system with a full-scale output of 9.375V and an accuracy of ±0.015%.

i. Determine the maximum deviation in the analog output due to the accuracy specification. (3 Marks)

ii. If the ideal output voltage is 6V, determine the possible range of the actual output due to this accuracy deviation? (3 Marks)

(b) The Fig. Q5(b) shows a certain logic gate. Describe its operation and develop its truth table and hence identify logic gate. (9 Marks)

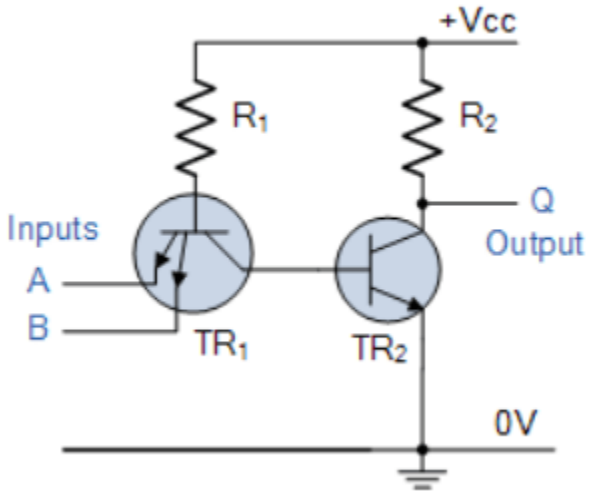


*Table Q4 (b)*